SEMICONDUCTOR DEVICE WITH SILICIDED SOURCE/DRAINS

Field of the Invention

This invention relates to semiconductor devices, and more particularly, to semiconductor devices with silicided source/drains.

Related Art

In common semiconductor manufacturing, semiconductor devices are made with lightly-doped drains at the junction with the channel and a relatively higher doped drain region used for making contact. The sources are made in the same way. The contact to the drain is made using a metal silicide. This contact is achieved by depositing the metal layer then reacting the metal layer with the silicon of the heavily-doped drain contact region to form a metal silicide contact region. The unreacted metal, which is located in the regions where there is no silicon, is then etched away with an etchant that is selective to the metal silicide. This metal silicide is then the contact point for the source and the drain of the semiconductor device.

One effective metal has been found to be cobalt. Cobalt is effective but has been found to be difficult to use for very small polysilicon dimensions. Thus, with cobalt there have been problems with achieving reliable and continuous cobalt silicide formed on narrow polysilicon lines. This is even called the "line width effect." Thus, other metals have been studied to overcome this problem. One promising metal is nickel. The use of nickel to form nickel silicide is effective for narrower line widths than have been found to be achievable for cobalt silicide. A difficulty with nickel silicide, however, has been the spiking of the nickel silicide to below the targeted depth in the

form of inverted pyramids. The nickel atoms tend to continue to extend along a downward path that may extend below the drain. When this spiking occurs, it has been found that that the silicide structure is nickel disilicide. The formation of this nickel disilicide has been particularly difficult to control for the semiconductor devices that are P channel transistors. Dopant atoms, such as boron that are smaller than silicon atoms, induce contraction of the silicon lattice. This causes the silicon substrate lattice to match with the lattice of the nickel disilicide thus causing nucleation of the nickel disilicide phase instead of the nickel monosilicide phase that would have formed had there been no lattice contraction.

Thus, there is a need for a technique for forming nickel silicide on source/drains that has improved manufacturability for P channel transistors.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

FIGs. 1-7 are cross sections of a semiconductor device at sequential stages in processing according to an embodiment of the invention.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description of the Drawings

In one aspect a relatively deep germanium implant and activation thereof precedes deposition of the nickel that is used to form nickel silicide. The activation of the germanium causes the lattice constant in the region of the implant to be increased over the lattice constant of the background substrate, which is preferably silicon. The effect is that the lattice so altered avoids formation of nickel disilicide. The result is that nickel silicide spiking is avoided. This is better understood with reference to the FIGs. and the following description.

Shown in FIG. 1 is a semiconductor device 10 comprising a semiconductor substrate 12, a gate 14 on a gate dielectric 16, and a liner 18 around gate 14 receiving a germanium implant. The result of the implant and subsequent anneal is the formation of modified lattice regions 20 and 22. Semiconductor device 10 is, in this example, being made into a P channel transistor. Substrate 12 is preferably silicon doped to N- so as to form an N well region. This may be achieved by starting with a bulk P- substrate and selectively doping active regions to N- for formation of P channel transistors in which case substrate 12 is a well region within a larger substrate. Liner 18 is formed by an oxidation step. An antireflective coating (ARC), which is present for other reasons, prevents oxidation on the top of gate 14 and is then removed. Regions 20 and 22 are adjacent to gate 14, since gate 14 acts as a mask during germanium implant that forms regions 20 and 22. The region in substrate 12 between regions 20 and 22 is where the channel of the P channel transistor is to be located. Regions 20 and 22, after being annealed, have a lattice that is stretched compared to a silicon-only lattice structure. The stretched lattice has a spacing that is larger than that of nickel disilicide, which makes formation of

nickel disilicide difficult. The germanium implant in the present embodiment is preferably at least 3Kev at a dose of at least 10 to the 13^{th} (1E13) atoms per centimeter squared. One example is 10Kev at 1E15 atoms per centimeter square. Preferably the energy should not exceed 50Kev, but it could be higher. The dose preferably does not exceed 1E17 atoms per centimeter square but could be greater than that. The anneal, which causes the activation of the germanium, is preferably between 900 and 1400 degrees Celsius. The activation can occur at an even lower temperature, such as 550 degrees Celsius. One example of an effective anneal is 1050 degrees Celsius for 5 seconds.

Shown in FIG. 2 is device 10 after formation of sidewall spacer 24 around gate 14 and a source/drain implant of boron to form source/drain regions 26 and 28 using gate 14 and sidewall spacer 24 as a mask. A boron implant may be in the form of boron difluoride. Most of the boron remains and most of the fluorine outgases during subsequent thermal processes. This implant is sometimes referred to as an extension implant. This forms the extension source/drain regions 26 and 28 that are at the interface with the channel of the ultimate P channel transistor that is formed. This formation of source/drain regions 26 and 28 are within modified lattice regions 20 and 22, respectively. But for the presence of regions 20 and 22, this formation of extension regions 26 and 28 is well known in the art of semiconductor processing.

Shown in FIG. 3 is device 10 after formation of sidewall spacer 30 around sidewall spacer 24 and a source/drain implant of boron to form source/drain contact regions 34 and 36 using gate 14, sidewall spacer 24, and sidewall spacer 30 as a mask. Sidewall spacer 30 may be a composite of more than one layer. For example this could be an oxide layer followed by a nitride layer. In this case, regions 34 and 36 extend below modified lattice regions 20

and 22. Especially in SOI substrates, there is also the possibility that the contact source/drain implant and the germanium implant will terminate at the interface of the semiconductor layer and the insulating layer that is below the semiconductor layer. These source/drain contact regions 34 and 36 are also known as deep source/drains and, but for the presence of modified lattice regions 20 and 22, the formation of source/drain contact regions 34 and 36 is well known in the art of semiconductor processing.

Shown in FIG. 4 is semiconductor device 10 after annealing the source/drain implants as shown in FIGs. 2 and 3. This activates these implants and has the effecting of expanding regions 26, 28, 34, and 36. The extension regions, source/drain regions 26 and 28, expand to be at least aligned to the edges of gate 14. The anneal will cause regions 28 and 36 and regions 26 and 34 to have a gradual change, if any, in doping concentration so they effectively merge into single regions. But for the presence of modified lattice regions 20 and 22, the process described for FIG. 4 is well known in the art of semiconductor manufacturing.

Shown in FIG. 5 is semiconductor device 10 after deposition of metal layer 38 that, in this example, is nickel. This layer 38 is in direct contact with source/drain regions 34 and 36, gate 14, and sidewall spacer 30.

Shown in FIG. 6 is semiconductor device 10 after a heating step to cause the formation of nickel silicide where nickel layer 38 is in contact with silicon. The result is the formation of silicide region 40 over and in source/drain region 34, a silicide region 42 over and in source/drain region 36, and a silicide region 44 over and in gate 14. These silicide regions 40, 42, and 44 are contacts that are effective for making an electrical connection as desired.

Shown in FIG. 7 is semiconductor device 10 after removal of the portion of layer 38 that was not silicided. This is achieved using an etchant, such as piranha, that is selective between the metal, which is nickel in this case, and the metal silicide, which is nickel silicide in this case. The device may then be subjected to an additional anneal to complete the silicide formation if so desired. This last anneal, however, may or may not be necessary depending on the process technology used in device fabrication. But for the presence of modified lattice regions 20 and 22, the steps described for FIGs. 5-7 are well known in the art of semiconductor manufacturing.

An alternative embodiment is to wait to perform the germanium implant until after the formation of the sidewall spacer that is used for the deep source/drain implant for making contacts. In such case the extension implant is performed prior to the germanium implant that forms the extension source/drain regions, the sidewall spacer for the deep source/drain implant is formed, and then the germanium implant is performed. This results in the germanium implant region being offset further from the channel than for regions 20 and 22 of FIG. 2. After the germanium implant and before the deep source/drain implant, the germanium implant is activated with a very short but high temperature anneal, which can be considered a non-diffusing anneal. Exemplary anneals are flash anneal and laser annealing. Flash annealing utilizes an arc lamp that provides very fast ramp rates for the heat. The intent is to increase the lattice constant in the area of the germanium implant without causing the extension regions to diffuse toward each other in the channel region. After formation of the modified lattice region, the deep source/drain implant is performed. The lightly-doped and heavily-doped regions can then be activated using standard techniques for that. The subsequent silicide formation

is thus over a region in which the lattice constant has been increased to avoid the nickel silicide spiking.

Thus, the regions of increased lattice constant, such as regions 20 and 22 which at least have portions in the source/drain contact regions, are useful in preventing spiking of nickel silicide and may be effective for preventing the spiking or the encroachment of other metal silicides such as cobalt silicide. The increased lattice constant regions in this described example are about 400 angstroms deep. It is preferred that the depth be greater than the silicide depth. Thus, the preferred smallest depth is at least the depth of the silicide. A greater depth than 400 angstroms should be effective as well. Activation of the germanium to form modified lattice regions 20 and 22 may occur at any time prior to formation of the silicide regions, but it is preferred that it occur before the implanting of the source/drain regions 26, 28, 34, and 36. Delaying the activation of the modified lattice regions 20 and 22 until after the source/drain implants causes competition with the source/drain implant dopants for the lattice sites. This can result in the lattice not being sufficiently modified to achieve the desired effect. Germanium has been found to be effective in avoiding spiking but other implanted materials may be effective as well. For example, other materials that may be effective include gallium, arsenic, indium, tin, antimony, thallium, lead, bismuth, zinc, cadmium, mercury, selenium, tellurium, and polonium. These materials all have a larger atomic radius than silicon and are in group II, III, IV, V, or VI, which are known to be able to be activated and occupy substitutional sites in a silicon lattice. In order to increase the lattice constant, any of these species or any combination of these species can be used to achieve the desired result.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, there may be other ways to modify the lattice constant of the substrate that has the needed characteristics. Also the source/drain contact regions may be in a region that is elevated above the plane of the substrate. These are called elevated source/drains. In such case the implant into the source/drain contact region to increase the lattice constant will be into the elevated region and the silicide will be formed on the elevated regions as well. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.